

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Richard Nathan, Dale E. Means, Jr.
Assignee: JigSaw Tek
Title: Integrated Circuit Package and Method For Fabrication
Serial No.: 10/077,211 Filing Date: Feb. 14, 2002
Examiner: Zarneke, David A. Group Art Unit: 2827
Docket No.: JIG006 US Confirmation No.: 3098

Santa Clara, California
April 23, 2003

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION

Dear Sir:

This is in response to the Office Action dated March 24, 2003. Specifically, in this Office Action, the Examiner required election of one of two groups. Applicants hereby elect, for further prosecution on the merits, the claims of Group I, namely Claims 1-8 and 18-29.

Please cancel Claims 9-17. Applicants reserve the right to prosecute these canceled claims in a divisional application in future.

Applicants respectfully bring to the Examiner's attention the documents cited in the attached Information Disclosure Statement (IDS). Applicants submit that no fee is due for entry of this IDS because an office action on the merits has not yet issued. However, if a fee should be required, please charge the deposit account 50-2263.

If there are any questions, please call the undersigned at 408/982-8200, extension 3.

**Via Express Mail Label No.
ER 205 699 576 US**

Respectfully submitted,

S. Omkar

Omkar K. Suryadevara
Attorney for Applicants
Reg. No. 36,320

SILICON VALLEY
PATENT GROUP LLP
2350 Mission College Blvd.
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210